Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS;**

1. **COMP 1**
2. **INPUT –**
3. **INPUT +**
4. **V –**
5. **OUTPUT**
6. **V +**
7. **COMP 2**

**.058”**

**.058”**

**MASK**

**REF**

**1**

**0**

**8**

**J**

**2 1 7 6**

**4**

**5**

**3**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V – (or Isolated)**

**Mask Ref: 108J**

**APPROVED BY: DK DIE SIZE .058” X .058” DATE: 12/8/21**

**MFG: NATIONAL THICKNESS .015” P/N: LM108A**

**DG 10.1.2**

#### Rev B, 7/19/02